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DESIGN, DEVELOPMENT AND TESTING OF A PROTOTYPE PRECISION ANGULAR POSITIONING CONTROL SYSTEM FOR A NEXT GENERATION MULTIPLEXED IMAGER

by
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December, 1994

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DESIGN, DEVELOPMENT AND TESTING OF A PROTOTYPE PRECISION ANGULAR POSITIONING CONTROL SYSTEM FOR A NEXT GENERATION MULTIPLEXED IMAGER

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ABSTRACT

This thesis presents a design for a precision angular position control system for use in a proposed multiplexed imager. The control system is designed to rapidly position a disk to within a tolerance of 2.5 μrad . Evaluation during the design phase shows an inherent trade-off between precision angular positioning and allowed angular velocities. Recommendations are provided for improving the time response of the control system. No testing was preformed to determine the actual positioning tolerance. In theory, the control system should have a tolerance of 0.65 μrad with a limiting angular velocity of 37 rpm.

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I. INTRODUCTION

A. BACKGROUND

The application of infrared (IR) detectors in the military has been growing steadily since they were first introduced. Today, this technology represents the best promise for developing new generations of target detection systems. IR detectors in night vision goggles were used very effectively in the Gulf War and have become vital too in successfully completing night time Navy search and rescue operations. Lawrence Livermore Laboratories has developed a projectile detection system using a two-dimensional focal plane array of IR detectors to determine the ballistic trajectory of an enemy projectile. Unfortunately, at very long wavelengths (far infrared to millimeter), the efficiency of focal plane array detectors decreases. For longer wavelengths, rapidly developing technologies are making the discrete, single-element IR detectors much more efficient, and therefore, more desirable for imaging applications.

B. TECHNIQUE

To use a discrete, single-element detector, the optical signal must either be raster scanned or spatially encoded (i.e., multiplexed) before being measured by the detector. The most common method for encoding the optical signal is to create a two-dimensional grid perpendicular to the optical axis of the instrument. Each discrete area on the grid, termed a pixel, receives a different sequence of encoding instructions, making each pixel an independent signal. After passing through the encoding grid, which is called a mask, the entire optical signal is then focused onto a discrete IR detector. Instead of measuring individual pixels with separate detectors like a focal plane array detector, the combined signals of all pixels are measured with a single detector. This makes use of the technique of multiplexing in its classical sense: "A multiplexed device is one which is capable of carrying or detecting several independent signals *simultaneously*, using only a single signal channel or detector [Ref. 1]."

Most encoding processes essentially transform the optical image into a two-dimensional type of Fourier series. Instead of using the traditional sine/cosine as the orthogonal basis set, the

technique of which this thesis is a part will use a digital orthogonal basis set known as Walsh functions. The straightforward application of Walsh functions is to use a Walsh-Hadamard encoding matrix that divides the two-dimensional grid into squares. Fancier image geometries could have shaped pixels in the shape of the desired recognition feature and could be used in military terminal target recognition applications. The physical approach in using the Walsh-Hadamard encoding matrix is to create an aperture that transmits the signal at locations where the Walsh-Hadamard matrix value is one, and block the signal where the Walsh-Hadamard matrix value is zero. Using this method, if an array of N x N pixels is wanted, then 2^N masks would be needed to fully encode the signal. By using the Kronecker product [Ref. 2,3] of two Walsh-Hadamard matrices, one that encodes along the vertical axis and the other which encodes along the horizontal axis, the total number of masks required to transform each dimension would be reduced to 2N. Finally, by reflecting the optical signal vice merely blocking (or absorbing) it, one physical mask can be made to represent both its own mask function and its inverse mask function. Since the reflected signal is used, the equivalent inverted mask from the physical set of masks can be removed. Thus, only N masks in each set of two sets of masks are required. This significantly reduces both the physical size and the complexity of the mask set.

C. PROPOSAL

A new design for a discrete, single-element IR detector imaging system using the technique of multiplexing has been proposed for development at the Naval Postgraduate School [Ref 4]. The desired target image enters the imaging system and is initially focused so that a real image is formed on the face of a disk containing the first encoding mask set. The resulting transmitted and reflected signals are redirected using mirrors to the second mask set, from different sides. The transmitted and reflected beams are then directed to separate IR detectors where they are measured. One detector will measure the combined signal that meets the condition of either having been reflected or transmitted by both masks. The other detector will measure the combined signal that meets the condition of having been reflected by either mask and transmitted by the other. To ensure the separation of the reflected beam from the incident beam on a mask, the incident beam is directed upon the mask at an angle slightly different from the normal to the

mask. This small deviation has been shown not to introduce a significant aberration in the image [Ref. 5]. Figure 1 shows a conceptual drawing of the proposed device [Ref 4].

D. EXPERIMENT

Physically, each mask used to encode the image is about 1 mm x 1 mm. In the proposed imaging system, a 64 x 64 pixel image is wanted: Therefore, 64 masks make up one complete mask basis set. The masks are laid out on a 5 inch diameter disk, about the size of a compact disk. For the experiment in this thesis, it was assumed that the centerpoint of each mask would be 6.0 cm from the disk center, each mask would have the same spatial orientation in relation to the center of the disk, and that the 64 masks were equally spaced around the disk. Since the mask set encodes 64 pixels, the internal pixel dimensions of the mask are on the order of 1 mm/64 = 15.6 μm. For good image accuracy, it is desired to position the masks to within 1% of their optimum aligned position. This requires a positional accuracy of 0.156 μm or an angular accuracy of 2.6 μrad.

In addition, each mask of one set must combine with each mask of the second set to form a complete image. Therefore, 4096 measurements must be made. A time delay of 1 second between measurements would require over an hour of measurement time to complete an image. Therefore, it is desired that the mask change position as rapidly as possible.

The research problem addressed by this thesis weighs those design trade-offs against one another, in order to design a precision rotational positioning system that is accurate to within 2.5 μrad, can rapidly position a disk from one angular position to the next in as short a time as possible, and can maintain the disk position within 2.5 μrad of a desired value without jitter.

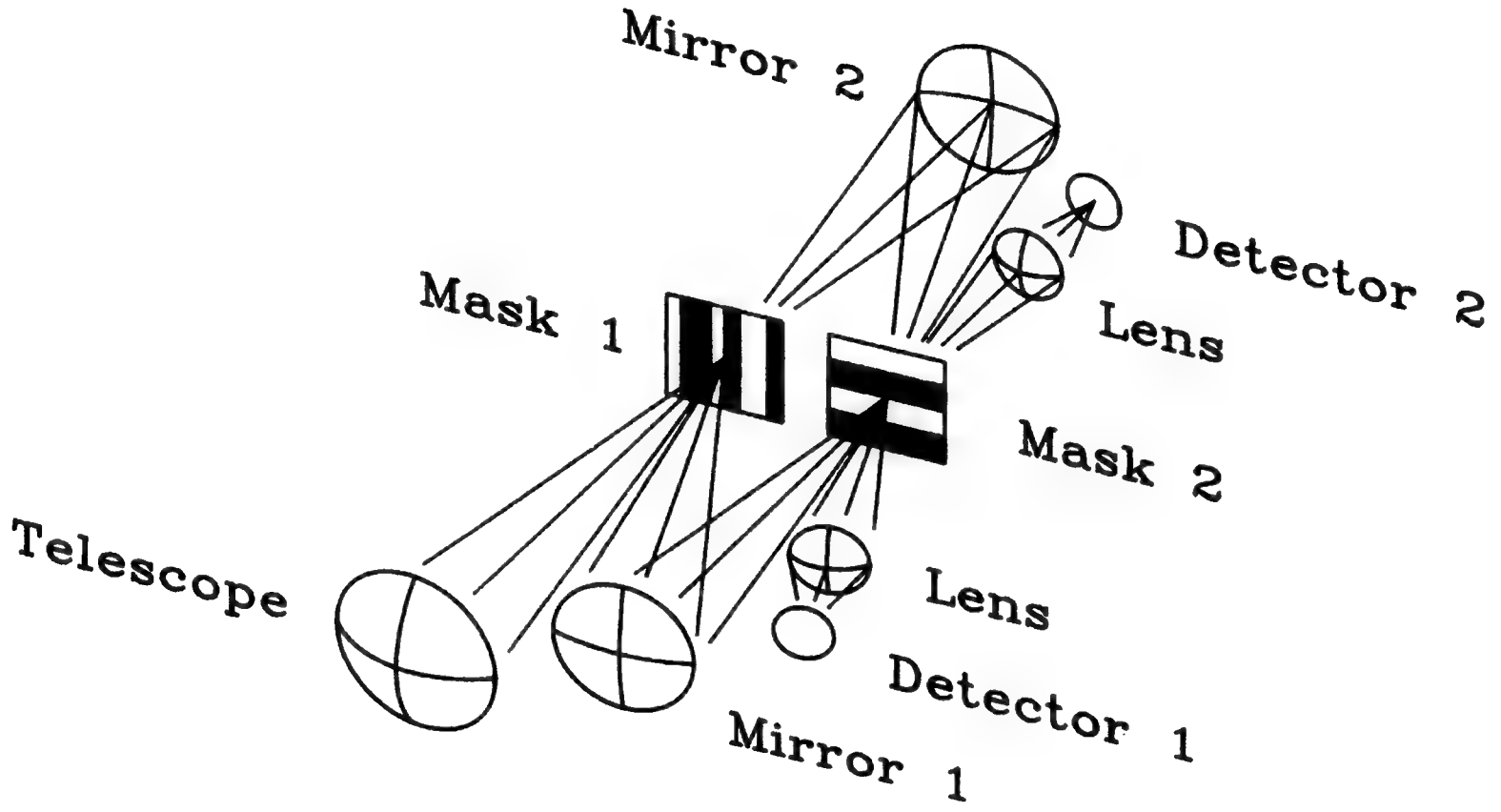

Figure 1. Basic optical configuration of a Kronecker product multiplexed imaging system.

II. THEORY

A. GENERAL OVERVIEW

The basic approach for the positioning control system was to use a position difference between the desired position and the measured position to develop an error signal, which would in turn drive a motor to rotate the disk to the desired position. A velocity measurement is used to provide a negative feedback to prevent overshooting the desired position. Figure 2 shows an example of a basic control system design. To physically realize this design, there must be several components with the ability to:

1) Accurately determine the disk position.
2) Determine the disk velocity.
3) Input the desired position.
4) Determine the appropriate error signal.
5) Apply the error signal into movement of the disk.

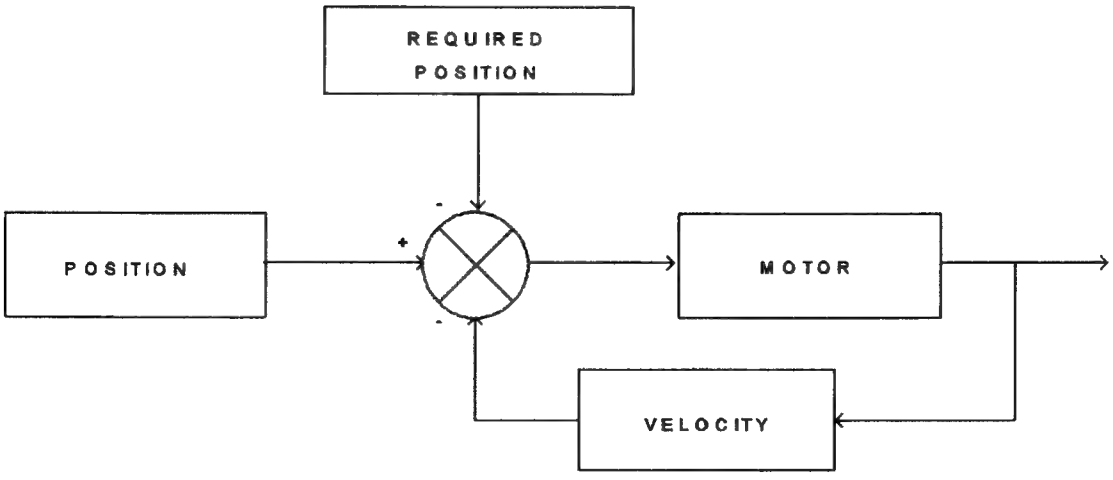

Figure 2. Basic position control system.

B. POSITION DETECTOR

The physical measurement of the disk's position is accomplished by a rotary encoder. There are many thousand of position encoders on the commercial market. Generally, the physical size of the encoder increases precision. To make the control system usable for its intended purpose, the size of the encoder is physically limited. The Canon laser rotary encoder K-1 was therefore selected for its small size and still relatively high degree of precision, approximately 77.6 μrad without electrical division. The output of the encoder is in the form of two sinusoidal waveforms with signal B delayed in phase with respect to signal A by 90° (i.e., quadrature signals). One complete revolution of the encoder generates 81,000 complete waveform cycles. A Z signal is also provided, which produces a narrow pulse each time the rotor passes a reference position. It is important to note that the output waveforms vary by angular position, not by time. Thus, if the encoder is stopped, the signals will be constant, but with an amplitude that corresponds to the encoder shaft rotational position. Thus, the relative phases of the waveforms contain the information needed to recover that angular position.

Having two signals 90° out of phase allows for the technique of adding in quadrature to exploit a signal, making the signal more accurate than the physical angular difference between two waveform peak values would permit. Adding in quadrature is achieved by multiplying each signal with a sinusoid waveform of a high frequency and adding the two products. In particular, signal A is multiplied by a cosine function of a known frequency, and signal B is multiplied by a sine function of the same frequency. The result is:

$$\cos(\omega(t))\cos(\omega_0 t) + \cos(\omega(t)-\frac{\pi}{2})\cos(\omega_0 t-\frac{\pi}{2}) = \cos(\omega(t))\cos(\omega_0 t) + \sin(\omega(t))\sin(\omega_0 t). \quad (1)$$

$\omega(t)$ represents the relative angular position of the encoder and $\omega_0 = 2\pi f$ is the angular frequency of the modulating signal. Applying simple trigonometric product identities, it can be shown that equation (1) yields:

$$\cos(\omega(t))\cos(\omega_0 t) + \sin(\omega(t))\sin(\omega_0 t) = \cos(\omega_0 t - \omega(t)). \quad (2)$$

To understand the results of this process, first consider the case where the encoder is stationary (i.e., $\omega(t)$ is a constant). By comparing the results of equation (2) to the reference modulating signal $\cos(\omega_0 t)$, it can be shown that the phase difference between these two signals is directly proportional to $\omega(t)$. By measuring the phase angle between the reference signal and the summed signal, it is now possible to directly determine the relative position of the encoder rotor with a particular waveform. This then provides the means of improving the effective precision of the encoder to well beyond the published value of 77.6 μrad.

Next consider the case in which $\omega(t)$ is changing. This causes equation (2) to change phase as a function of time in relation to the reference signal, $\cos(\omega_0 t)$. Each time that $\omega(t) = n2\pi$, where n is an integer, the two signals will be in phase. By keeping track of how many times the modulated signal passes through the "in phase" condition (i.e., counting n), it is possible to determine how many of the 81,000 waveforms the encoder rotor has passed through. This is the basic theory behind the comparator/counter circuit shown by Barbour [Ref. 6], and shown in revised form in Figures 10 and 11. Each time the reference signal passes its maximum value, the counter circuit counts up by one, and each time the encoder signal passes its maximum value, the counter circuit counts down by one. If the value of $\omega(t)$ passes an integer value of 2π in the positive direction, there will be two count up pulses from the reference signal before a count down pulse it generated. Effectively, the counter has counted up as the encoder moved to the next waveform. Conversely, if $\omega(t)$ passes an integer value of 2π in the negative direction, there will be a down pulse immediately after one up pulse, and a second down pulse before another up pulse is generated. Thus, the counter has counted down one.

The second point to observe from the case where $\omega(t)$ is changing is that the frequency of the modulated signal is no longer ω_0, but a new value. This becomes of concern if a filter must be applied to the modulated signal.

In the practical construction of a pulse detection system, the encoder signals are not multiplied with sinusoidal signals, but are modulated with square waves. The square wave can

be represented as a Fourier series expansion of sine waves with integer values of the original frequency. Each component of the series expansion can be combined with the encoder signal as in equation (2), forming a signal that looks like $\sum_N A_N \cos(N\omega_0 t - \omega(t))$. The unwanted signals are easily filtered out with a bandpass filter, but this puts an upper limit on how fast $\omega(t)$ can change.

In designing of the pulse count system, ω_0 was chosen to be 6.38×10^3 s^{-1}. The limits of the bandpass filter were set to $\frac{1}{2}\omega_0$ and $\frac{3}{2}\omega_0$. Therefore, the maximum angular velocity allowed for $\omega(t)$ would be 3.14×10^3 s^{-1} or 37 rpm for the encoder shaft. This places a minimum time delay between mask changes of 10 msec.

C. CONTROL SYSTEM DESIGN

Once the position detector is designed, a microcomputer can be programmed to provide all the other functions necessary to generate an error signal. The position detector sends a new position update to the microcomputer every millisecond. Since the microcomputer knows the time interval between successive positions, it is able to determine the encoder velocity. A new desired position is sent the microcomputer by an external source, and a new error signal is generated by summing the difference between the desired value and the present position with the velocity signal, properly weighted to ensure the system is critically damped. The resultant error signal is then sent to the motor via a digital-to-analog conversion circuit. The motor then drives the mask to the new desired position.

III. EXPERIMENTAL DESIGN

A. GENERAL APPROACH

As described in Section II, the experimental apparatus consists of several parts:

1) The pulse counter.

2) The microcomputer.

3) The motor drive circuitry.

4) The associated interfaces.

A schematic of how these components are connected is shown in Figure 3.

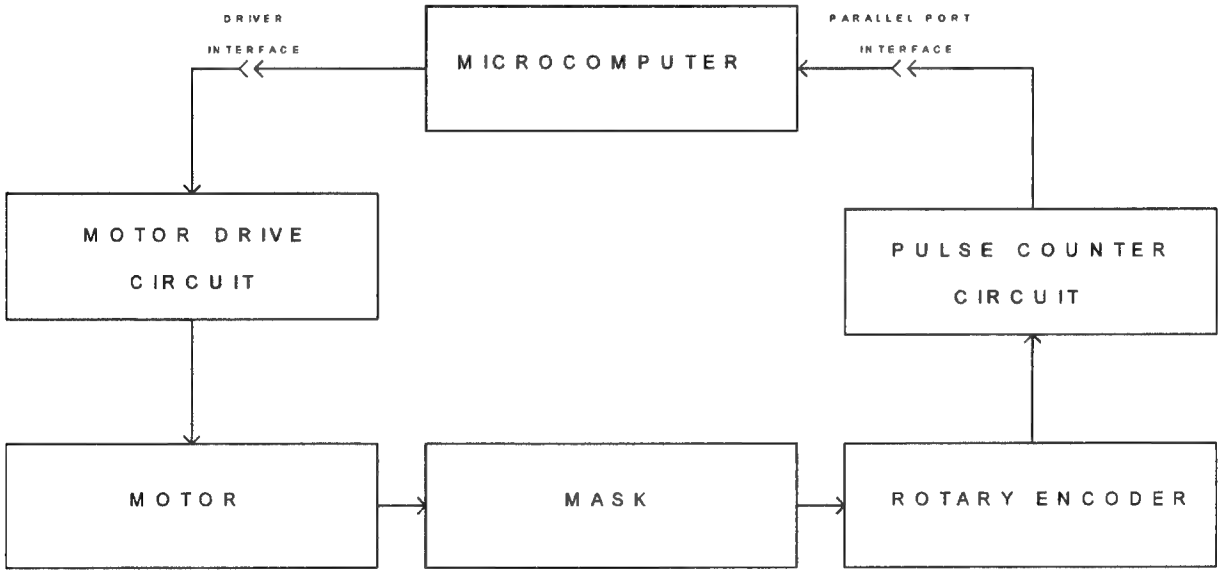

Figure 3. Schematic diagram of components in a position control system.

1. Pulse counter

The pulse counter consists of a modular design that processes the two signals generated by the rotary encoder and displays a numerical position in terms of which of the 81,000 waveforms corresponds to the encoder's position. A second display shows the relative position within a waveform. A schematic of the pulse counter is shown in Figure 4.

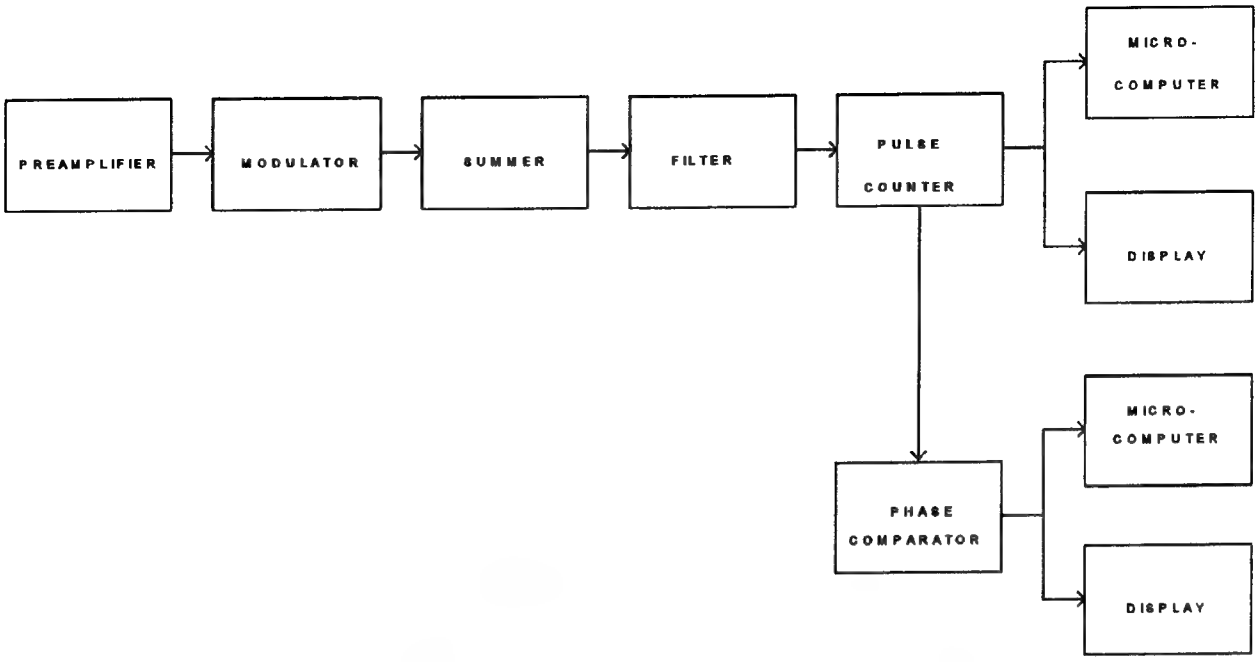

Figure 4. Schematic of pulse counter circuit.

The signals from the encoder are first passed to a modulator which multiplies the signals by the desired square waves. The resulting signals are then summed and passed to a filter which removes the harmonic frequencies. Next, the signal is passed to the comparator/pulse counter, where the whole number of cycles that encoder rotation has produced is counted. The comparator/pulse counter generates a binary output that is passed to the microcomputer via a parallel bus. The counter also generates a signal that can be displayed via LCDs. Finally, the up and down count signals from the comparator/pulse count circuitry are sent to the phase differentiator, which can determine the relative phase position of the encoder within each waveform to improve overall precision. This phase signal is also in the form of a digital output which is sent to a microcomputer, and a digital display signal for LCDs.

a. Clock circuitry

The clock circuitry provides the required signals for the modulating circuitry and provides for overall synchronous operation throughout the pulse counter circuitry. Figure 5 shows the design of the clock circuitry. A 4 MHz clock oscillator provides the initial stable frequency. The clock oscillator must be four times the desired modulating frequency to generate

a modulating signal for encoder signal B that is 90° out of phase with the modulating signal for encoder signal A. A 4 MHz clock oscillator was chosen because of availability and ease of dividing down the clock pulses.

After the clock signal is reduced to 400 kHz by a divide by ten counter, two quad J-K flip-flops generate four 100 kHz square wave signals that differ in phase by 90°. Two signals that differ by 180° are used to modulate channel A and the other two signals with a 180° phase difference modulate channel B. These signals are labeled CLKA1, CLKA2, CLKB1, and CLKB2 respectively. CLKA1 serves as the reference clock signal throughout the pulse counter.

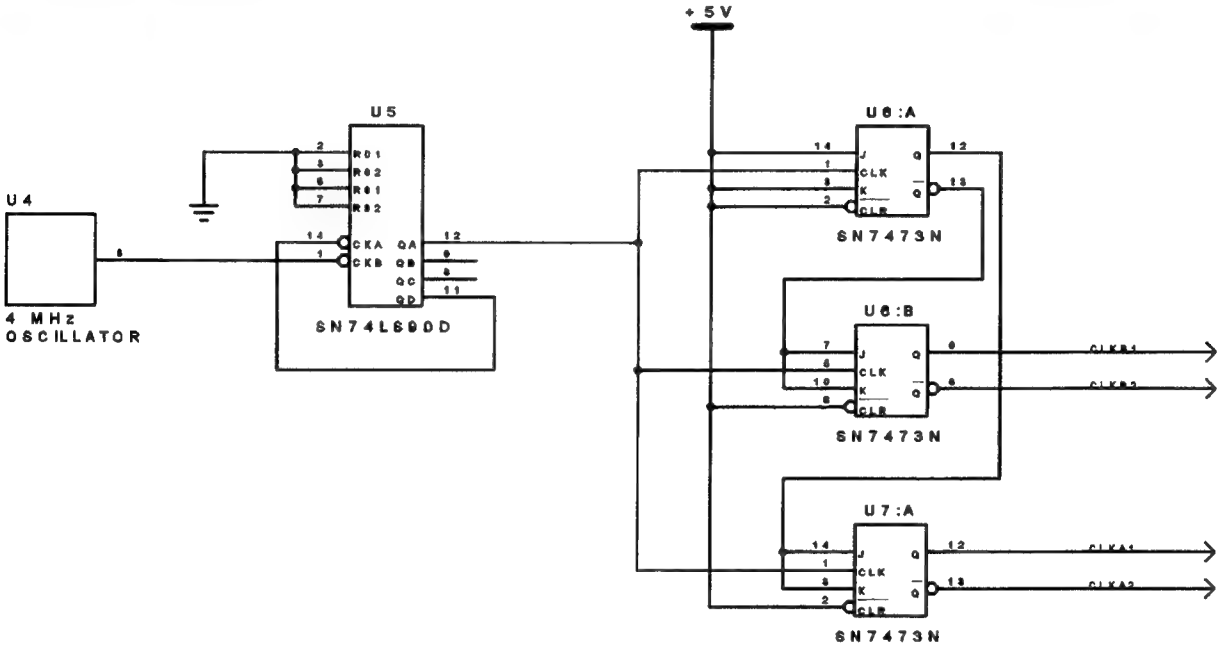

Figure 5. Clock circuit.

b. Modulator

The amplitude modulation circuitry is based on a design published by Stout [Ref. 7]. Figure 6 shows a schematic diagram of the modulator in its final form. The encoder signals A and B are sent to conditioning operational amplifiers at the input of the modulator via preamplifiers shown in Figure 7. The operational amplifier ensures that the encoder signal is properly zeroed and has a maximum voltage of 2 Vpp. The primary use of the conditioning amplifier is to allow encoders that emit square wave signals to work in this circuitry. It is not

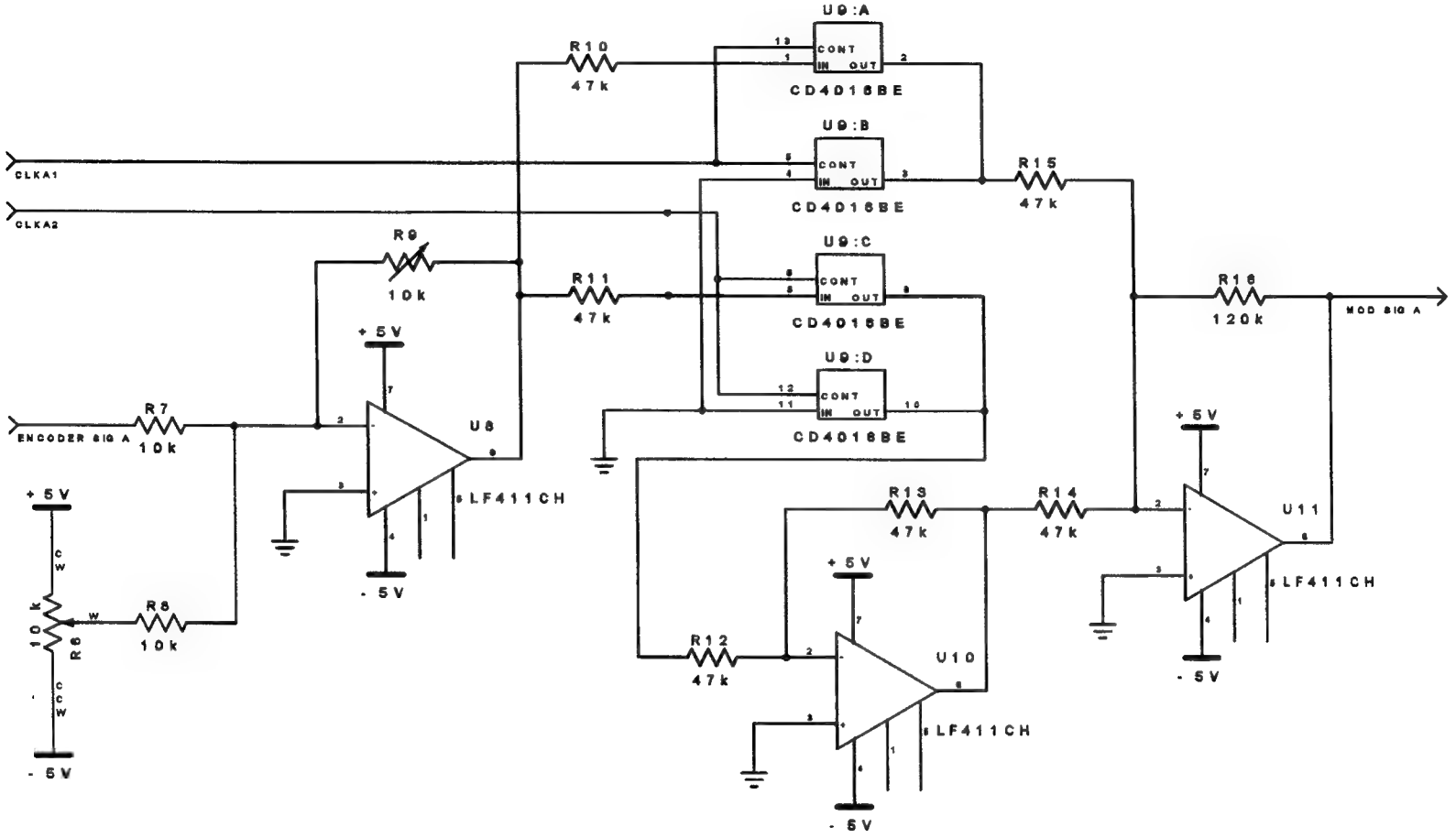

Figure 6. Amplitude modulation circuit.

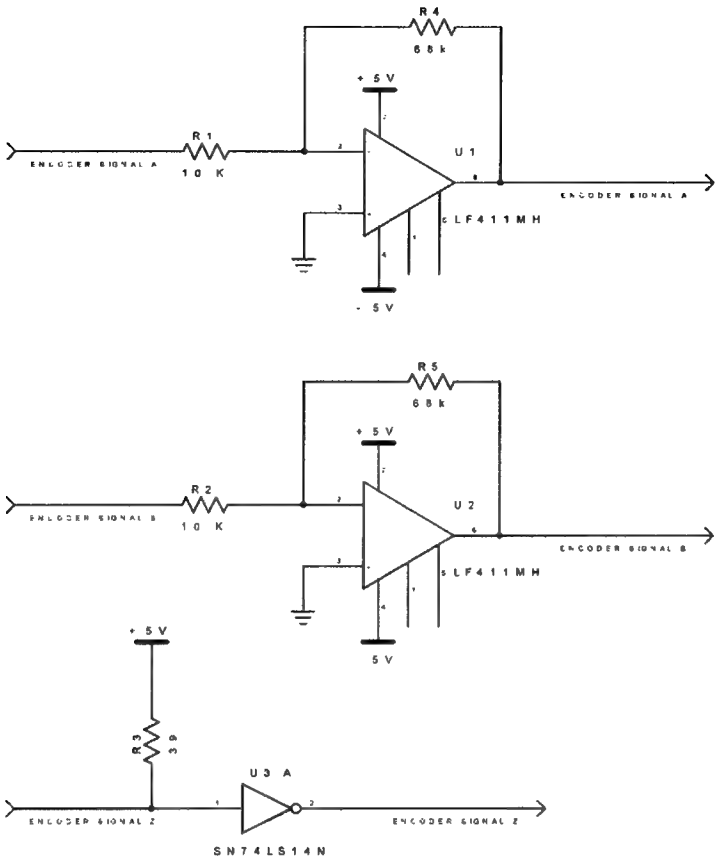

Figure 7. Encoder signal preamplifiers

strictly required with sinusoidal encoders.

The analog bilateral switches are driven by the 100 kHz square wave signals supplied by the clock circuitry. One signal controls two switches, and the inverted signal drives the other two switches. The output of the conditioning amplifier is connected to the inputs of two switches, one controlled by each of the clock signals. The inputs to the other two switches are connected to ground. The outputs of the switches connected to the conditioning amplifier are jumpered to the output of the switches connected to the ground signal controlled by the opposite clock signal. Thus, when a clock signal closes the switch that passes the output of the conditioning amplifier, the switch which connects the output to ground is opened. The outputs of the two sets of

switches is then a square wave with a zero amplitude for one-half the waveform, and an amplitude equal to the output of the conditioning amplifier for the other half. Note that the amplitude of the pulses can be either positive or negative. Finally, one of the two pulsed signals is inverted by a unity gain inverting operational amplifier. The two signals output by the switches are summed together by a summing amplifier to form an equivalent of the input encoder signal modulated by a 100 kHz square wave.

The initial design outlined by Stout used LM339 comparators for the operational amplifiers. During construction of the modulation circuitry, the measured output signal resembled a flattened triangular wave, and did not represent the desired waveform. It was determined that the original circuit was designed to run at 1 kHz, and the LM339 comparators could not provide the correct gain at the higher frequency used in our circuit. Therefore, LF411 operational amplifiers were exchanged into the circuit to provide better gain response. After the exchange, the output waveform exhibited the expected pulse shape except for a small distortion that lasted for about a microsecond on the leading edge of each pulse. This distortion is attributed to propagation delays and switch bouncing in the operation of the bilateral switches. Since the signal is subsequently filtered, it was considered that these small distortions may be insignificant.

c. Filter

Between the modulator circuit and the filter is a summing amplifier that sums the modulated A and B signals in quadrature, as shown in Figure 8. The filter was designed as a sixteen pole Butterworth band-pass filter using the designs shown by Horwitz and Hill [Ref. 8]. Figure 8 shows the schematic for the filter. The large number of poles were chosen to ensure a flat gain for the desired band pass region and a rapid roll off at the band rejection frequencies. The band-pass frequencies required are one-half and three-halves the modulation frequencies, or 50 kHz and 150 kHz, respectively. Following construction of the filter, it was tested using an HP4194 impedance analyzer to ensure that its transfer function was correct. Figure 9 shows the frequency response of the band-pass filter.

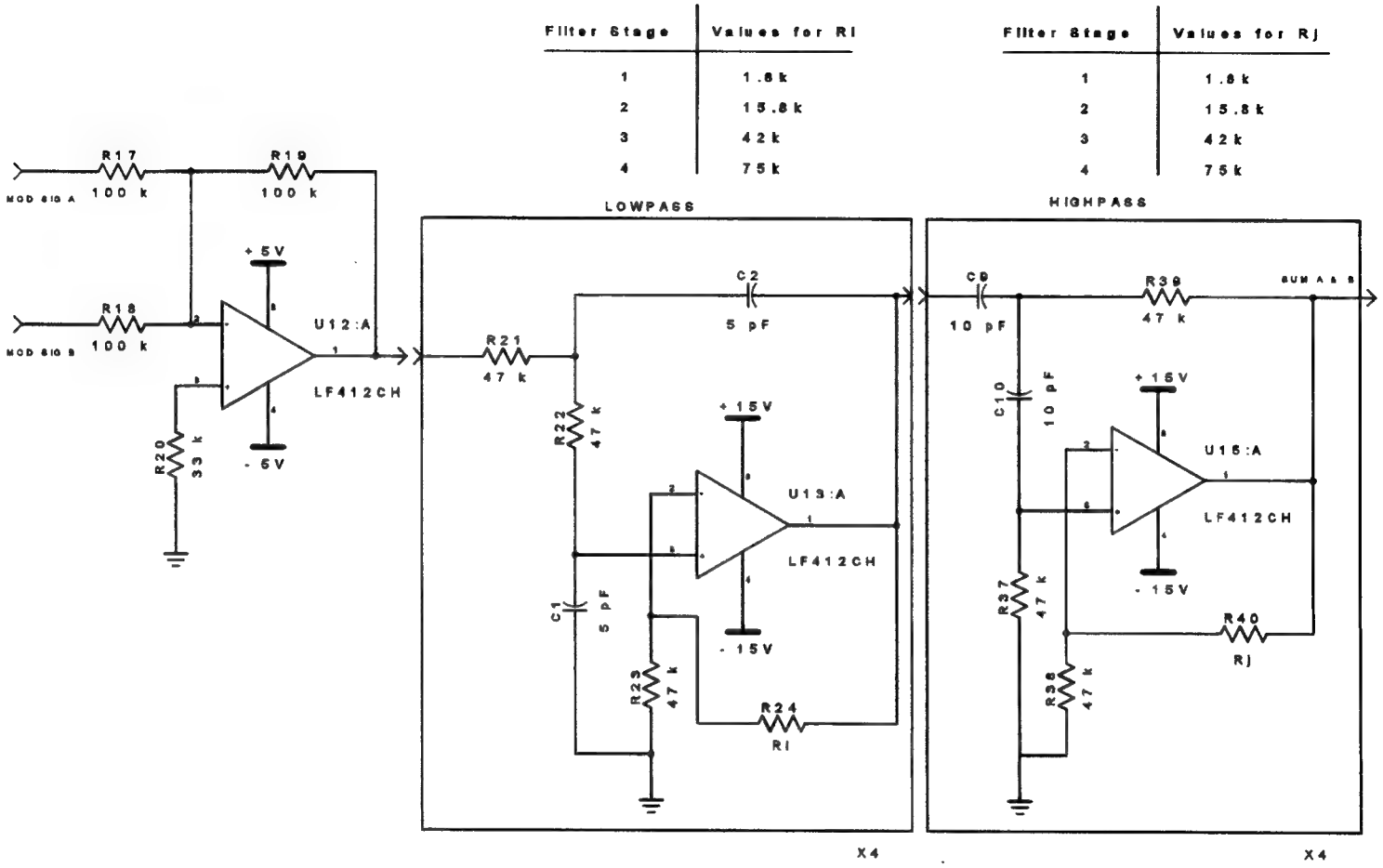

Figure 8. Summing amplifier and filter.

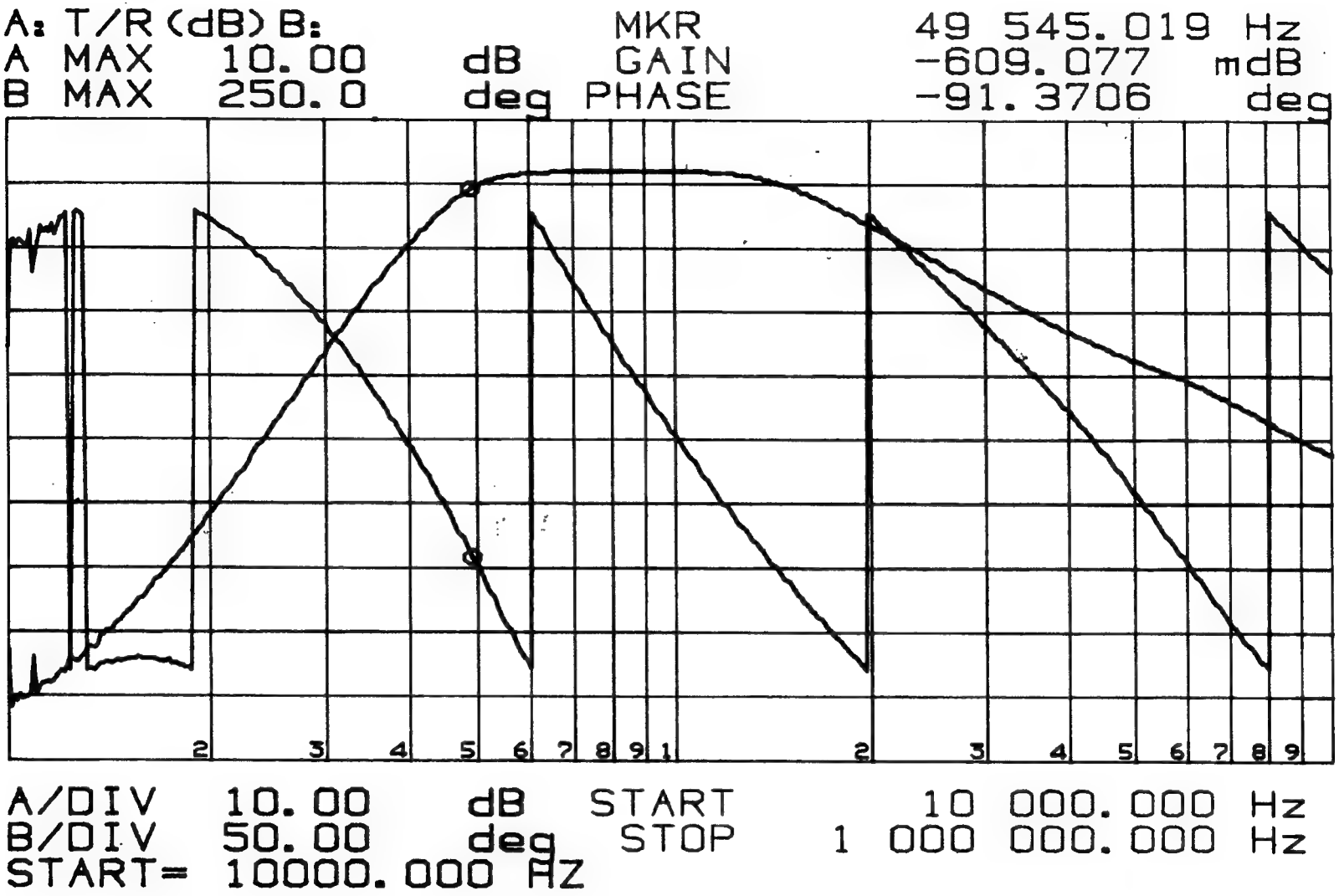

Figure 9. Frequency respnse of band-pass filter

d. Phase comparator/pulse counter

Figures 10 and 11 show the diagram for the phase comparator/pulse counter, modified from the design presented by Barbour [Ref. 6]. In the comparator/pulse counter circuit, the filtered signal is sent to a Schmitt trigger which conditions the SUM A & B signal. The Schmitt trigger provides a high TTL signal when the amplitude of the signal rises higher than a threshold value, and it then returns a zero signal when the signal falls below a lower threshold value. As designed, the Schmitt trigger provides a TTL pulse when the SUM A & B signal reaches its maximum amplitude. The reference 100 kHz clock signal (CLKA1) does not need conditioning by a Schmitt trigger, since it is already a TTL-compatible square pulse.

The comparator/pulse counter uses a pseudo-digital push-pull method to keep track of how many pulses the encoder rotation has produced. The pulse counting is accomplished by a series of binary up/down counters. The circuit reference signal will always send an up pulse to the counters every 10 μsec. If the rotor is stationary, a down pulse will be generated at some time between the up pulses, but always interleaved with the up pulse, so there is no net change in pulse count during the reference clock period. As the rotor starts to move in reverse, the frequency of SUM A & B increases, and during some of the 10 μsec intervals, two down pulses occur between consecutive up pulses, causing a net down count for the pulse counter. Conversely, if the encoder rotates forward, the SUM A & B frequency goes lower, causing some intervals between up pulses not to have an associated down pulse. This leads to a net up count.

The HC123 square pulse generators form the heart of the conflict avoidance circuitry. Because the up/down counters have a finite propagation delay time (10 nsec), it is necessary to delay the down count until the up count has fully cleared the counters. The conflict avoidance circuitry senses when an up pulse is sent to the counters and blocks the down pulse from being sent for 500 nsec. The D-latch following the Schmitt trigger ensures that the down pulse remains available until after it has caused the counters to count down, at which time the D-latch will clear.

The buffers are used to provide the microcomputer with a steady signal that does not show the constant up/down pulse toggling. The clock function for the buffers is controlled by the up count pulse. Therefore, the buffers only change their value every 10 μsec and always at the same phase relationship with the reference clock signal.

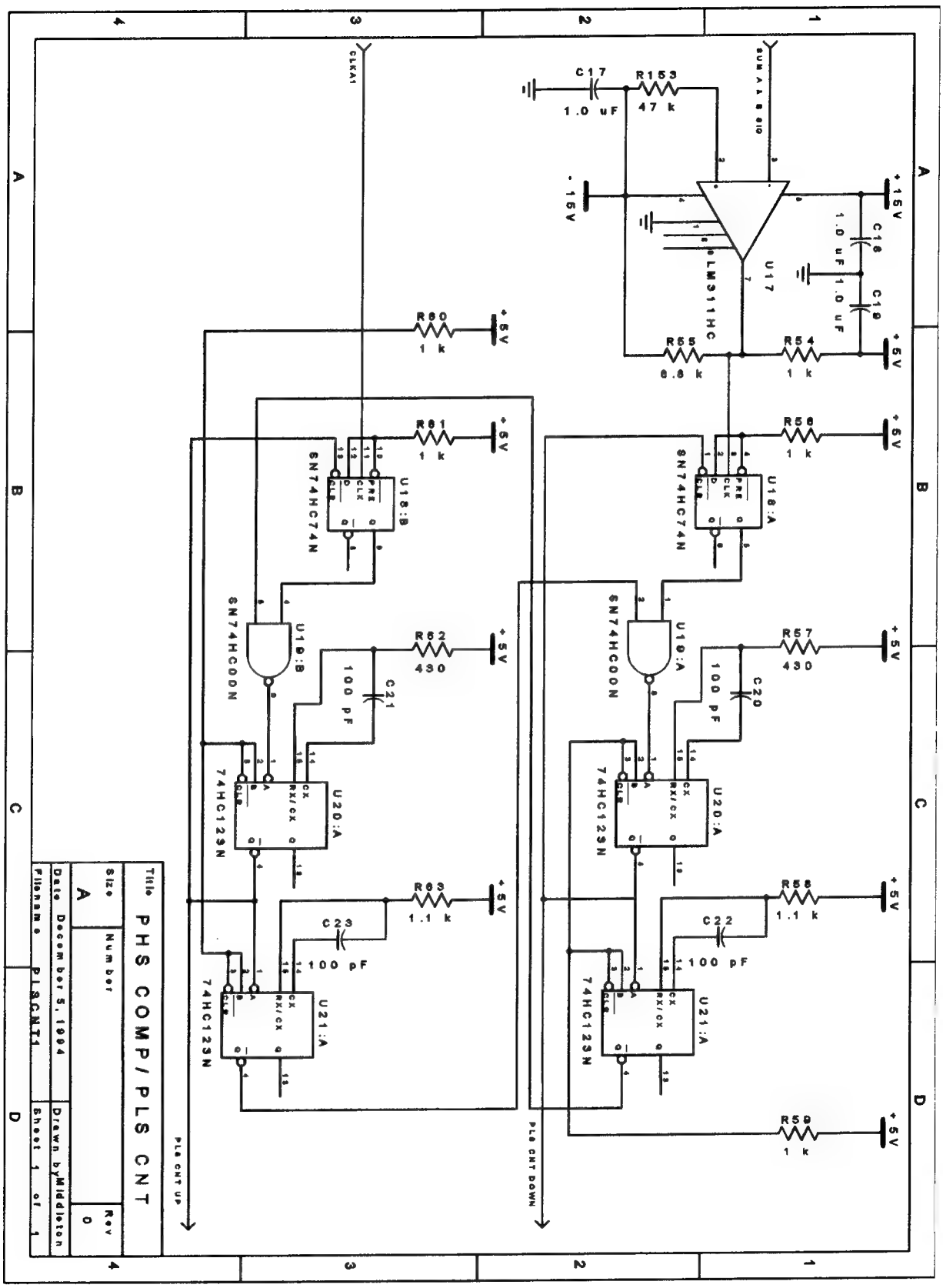

Figure 10. Phase comparator/pulse counter sheet 1 of 2.

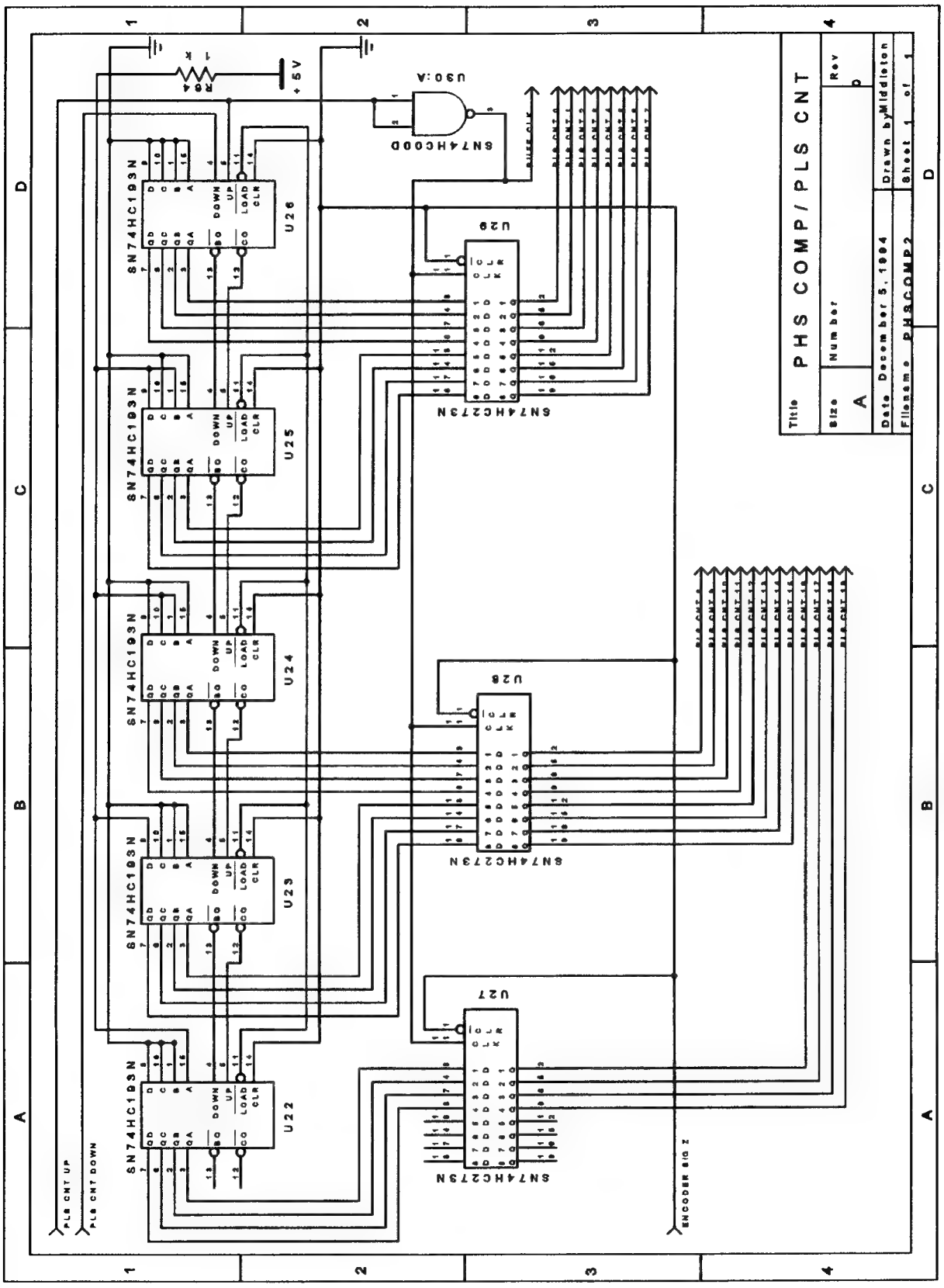

Figure 11. Phase comparator/pulse counter sheet 2 of 2.

The final feature of the phase comparator/pulse counter is its load function. The load data programmed into the five binary counters load a preset value of 100,000 into the counters. This is the nominal reference position of the encoder ,and it allows the counters to count up or down 81,000 pulses smoothly before another load pulse is received. The load pulse is received from encoder signal Z.

e. Pulse LCD indicating circuitry

To provide a means to easily determine the position of the encoder, LCD indicating circuitry is provided. This is shown in Figures 12 and 13. This circuit simply takes the up and down count pulses from the comparator/pulse counting circuitry and applies the count pulses to BCD up/down counters. The decade counters send the pulse count signal to buffers used to reduce visible jitter. The count is then sent to LCD 7-segment drivers that in turn sends the required signals to display 6 digits. The BCD counters are also loaded with a value of 100,000 and will reset the displayed counter value to 100,000 each time the encoder signal Z is generated.

f. Phase differentiation circuitry

The phase differentiation circuitry provides a means to determine the relative phase difference between the reference signal and the SUM A & B signal. Figure 14 shows a schematic of this circuit. The reference pulse (count up) and the pulse from the SUM A & B signal (count down) are taken from the phase comparator/pulse counter circuitry prior to the conflict avoidance section and sent to short (200 nsec) square pulse generators. The resulting pulses are then supplied to the clock functions for two D-latches. When the reference pulse clocks the first D-latch, the resulting signal goes high. When the SUM A & B pulse clocks the second D-latch, it forces the first D-latch to reset, thus dropping the resulting signal low. The pulse that is generated is a square pulse with a length directly proportional to the time difference, and hence the phase difference, between the two signals. The pulse is then sent to a logic AND gate and combined with a high frequency clock signal to generate a series of pulses. In this design, a 12 MHz clock oscillator is used. The output of the AND gate is a number of pulses proportional to the length of the phase difference pulse. For a circuit frequency of 100 kHz, a maximum of

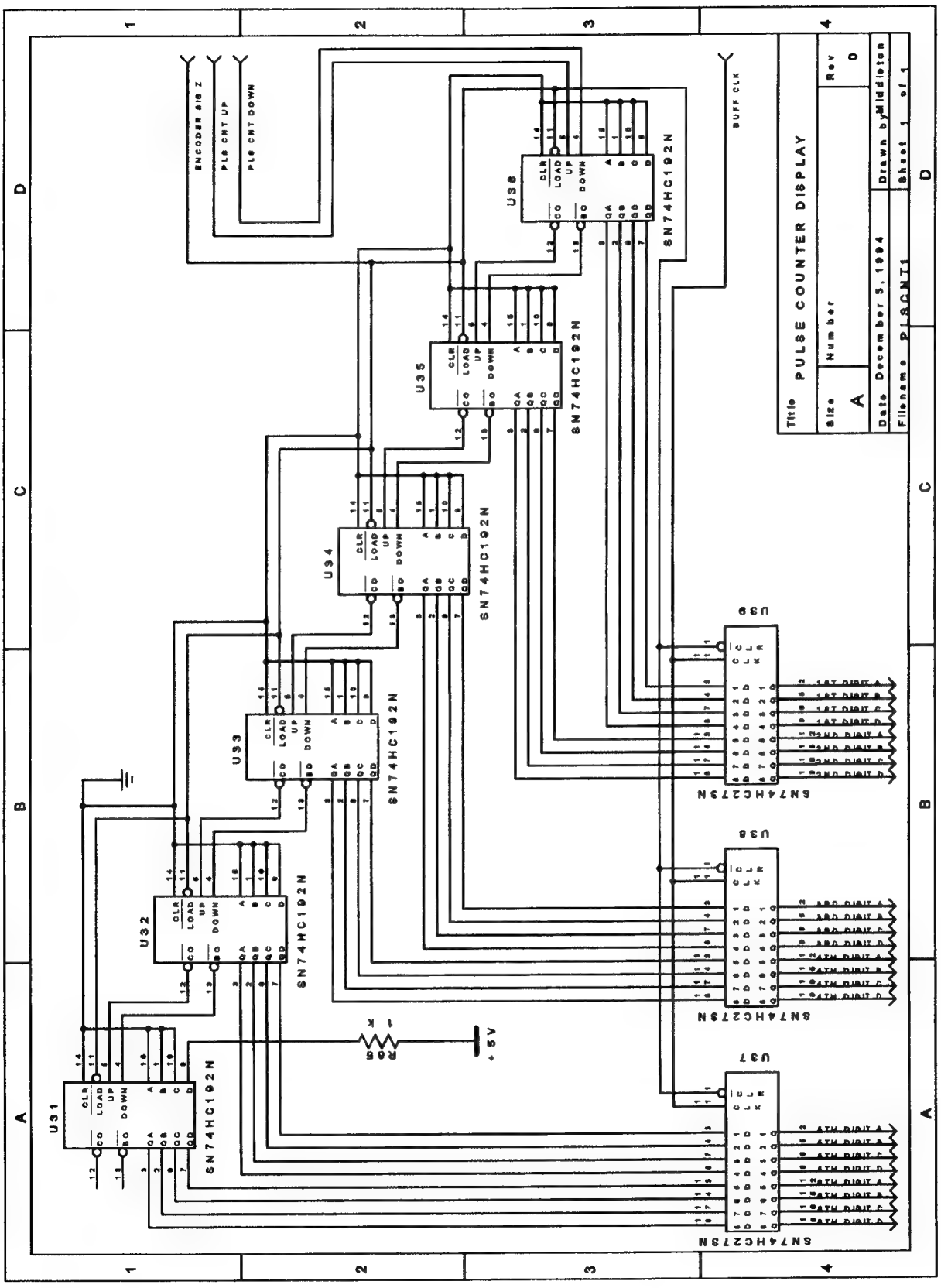

Figure 12. Pulse LCD indicating circuit sheet 1 of 2.

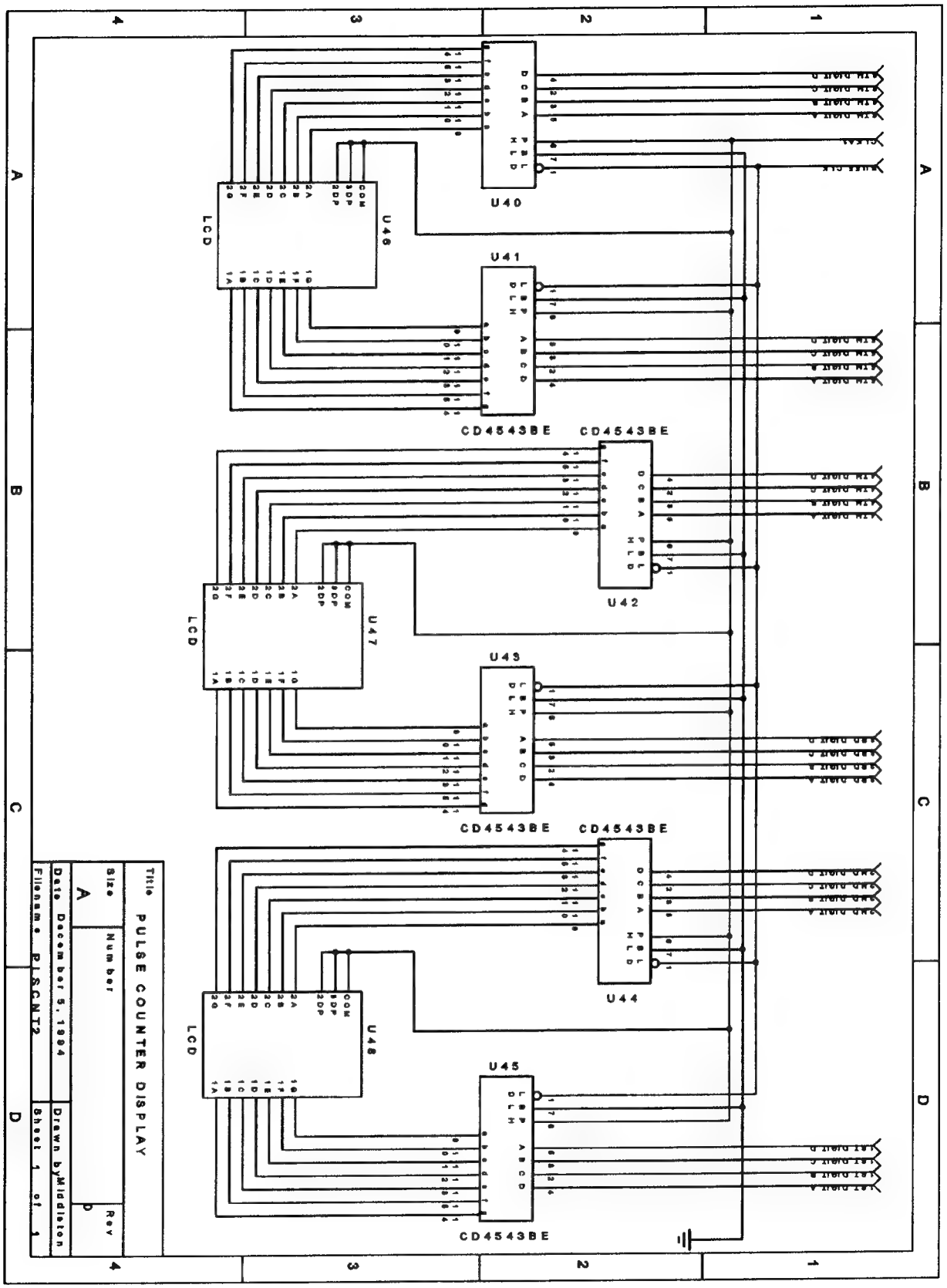

Figure 13. Pulse LCD indicating circuit sheet 2 of 2.

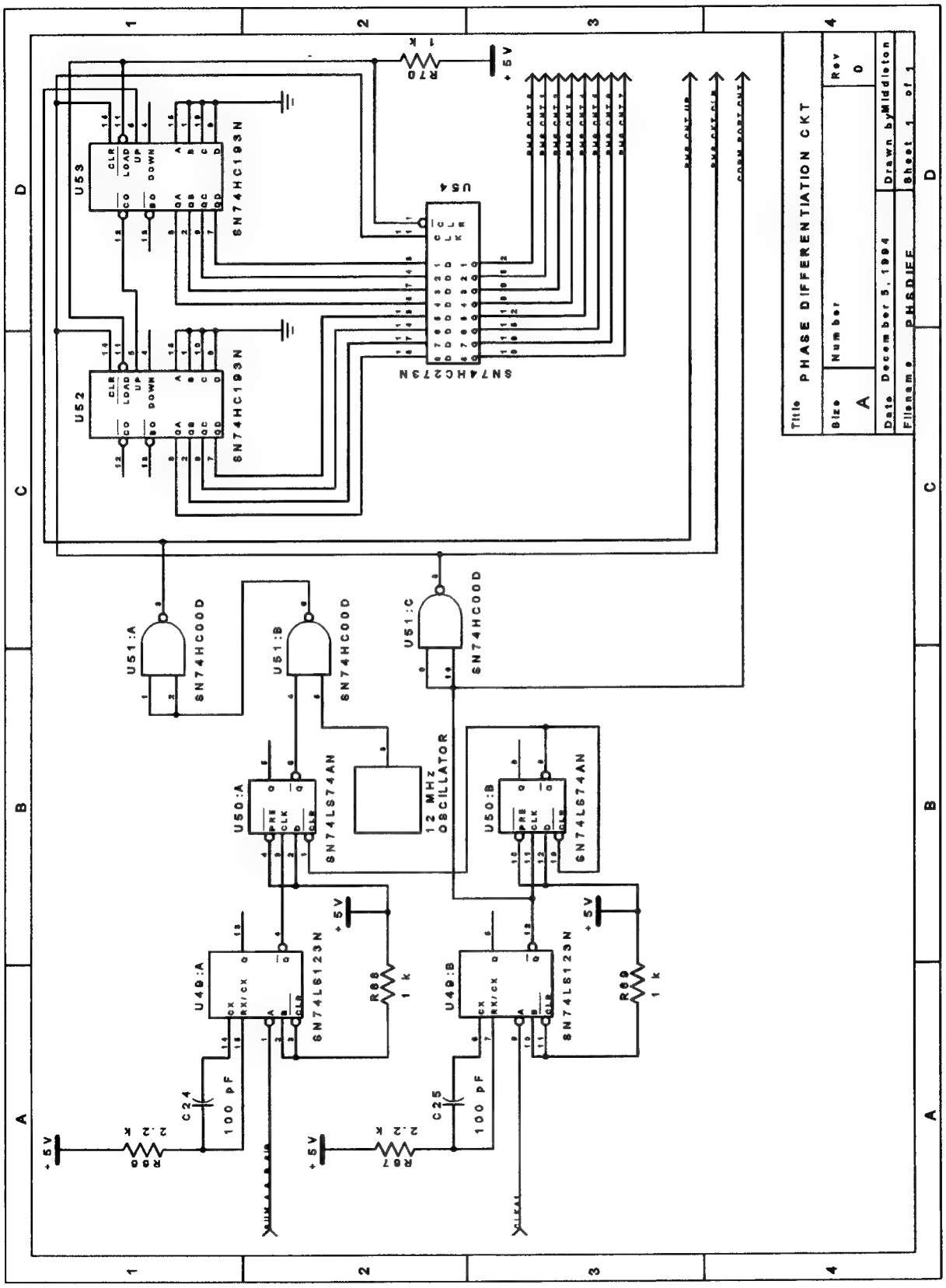

Figure 14. Phase differentiation circuit.

120 pulses can fit in the phase difference pulse. The result is that one encoder waveform can be subdivided into 120 equal segments, thereby increasing the precision of the encoder. After, the pulses are generated from the AND gate, they are sent as up counts to a series of two binary up/down counters. It is unnecessary to develop or to count a down pulse, since only the number of pulses in each pulse train is desired. The results of the counters are supplied to a buffer that is clocked to the reference signal, so that only the end count is latched on the buffer. The reference signal also clears the counters to let them count up from zero for the next cycle.

g. Phase differentiation LCD indication circuitry

In much the same way as the pulse count circuit operates, the phase differentiation circuitry takes the up pulses input into the binary counters, and inputs it into a set of three BCD up/down counters. These counters then supply the phase count to the buffers, which in turn supply a signal to the BCD 7-segment LCD drivers which then display 3 LCD digits. This is shown it Figure 15.

2. Microcomputer

The microcomputer is a Z-World "Tiny Giant," which runs a variant of C entitled Dynamic C. The microcomputer has two 8-bit parallel ports, four high voltage driver ports, three analog ports, and two serial ports. One serial port is generally dedicated to communicate with the host computer, which allows the operator to control the microcomputer externally. Data from the pulse counter and phase differentiator must be passed to the microcomputer via the parallel ports, and the driver ports must be used to develop the motor drive signal. Finally, the microcomputer must be programmed to read in an encoder position, compare it to the previous position to determine velocity, compare the position to the desired position input at the terminal, develop an error signal, and output the motor drive signal.

a. Parallel port interface

The total number of bits representing the encoder position is 26. This greatly

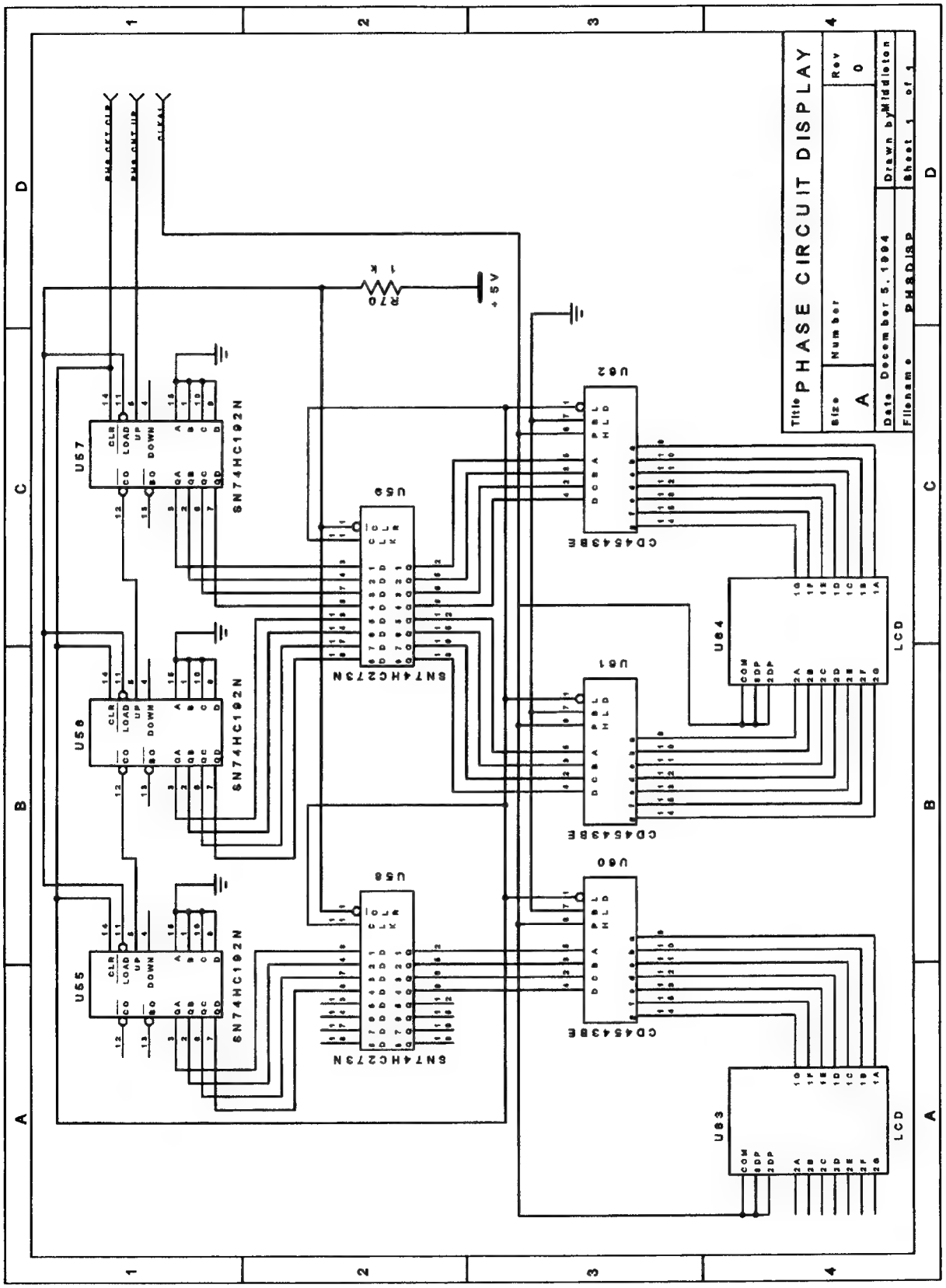

Figure 15. Phase LCD indicating circuit.

exceeds the capacity of the Tiny Giant's 16-bit parallel port. Therefore, the signal must be multiplexed. In addition to the 26 bits of data, there must be an interrupt signal which will tell the microcomputer when to read a position, and an output from the microcomputer to shift the multiplex for the second set of data. Figure 16 shows a schematic of the parallel bus interface.

Bit 7 of port B was designated the position ready strobe. The reference clock signal is passed through two inverters to allow a small time delay following the clocking of the buffers. The reference signal is then conditioned into a 500 nsec square pulse and sent to multiplex channel A side connected to bit-7 input of port B. During testing of the circuit, it was determined that clocking positions into the microcomputer every 10 μsec was over-taxing the microcomputer. Using two divide by 10 counters, the strobe signal was reduced to one count every millisecond. Bit 6 of port B was designated the output bit that would request multiplex channel B. The output of bit-6 port B was wired directly to the select contacts for the multiplex lines. The other fourteen lines of the parallel bus were connected to the output of fourteen multiplex channels. The eight bits from the phase differentiation circuitry were sent to the first 8 least-significant bit multiplex lines. The first six least-significant bits of the pulse counter were sent to the rest of the available A channels. The remaining 12 most-significant bits of the pulse counter were then sent to the first twelve channel B multiplex lines. The remaining two channel B lines were wired to ground, as was the channel B line opposite the microcomputer handshake signal. The multiplex strobe lines were wired to ground to ensure that the most current values of the buffers were always sent to the microcomputer.

b. Motor drive circuitry

The motor drive output signal from the microcomputer was in a digital form, but to smoothly operate the motor, the signal had to be converted to analog and had to swing both positive and negative in order to drive in both the forward and reverse directions. Figure 17 shows the motor control interface. The four high voltage drive outputs were connected to a quad bilateral switch via pull-up resistors. When a driver channel was tied to ground, the output value of the port was zero. When the driver port went high, it was no longer connected to ground, and

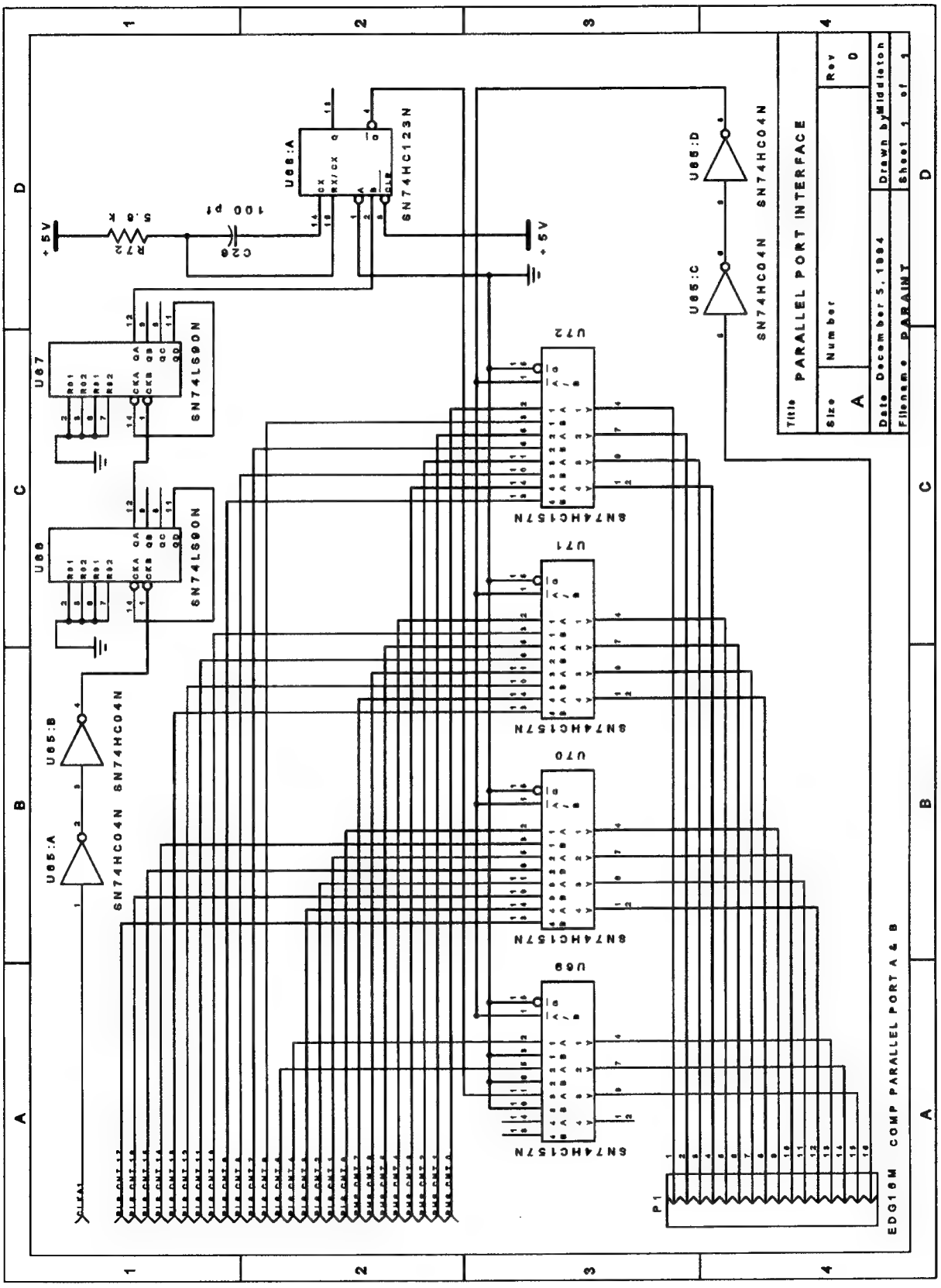

Figure 16. Parallel port interface.

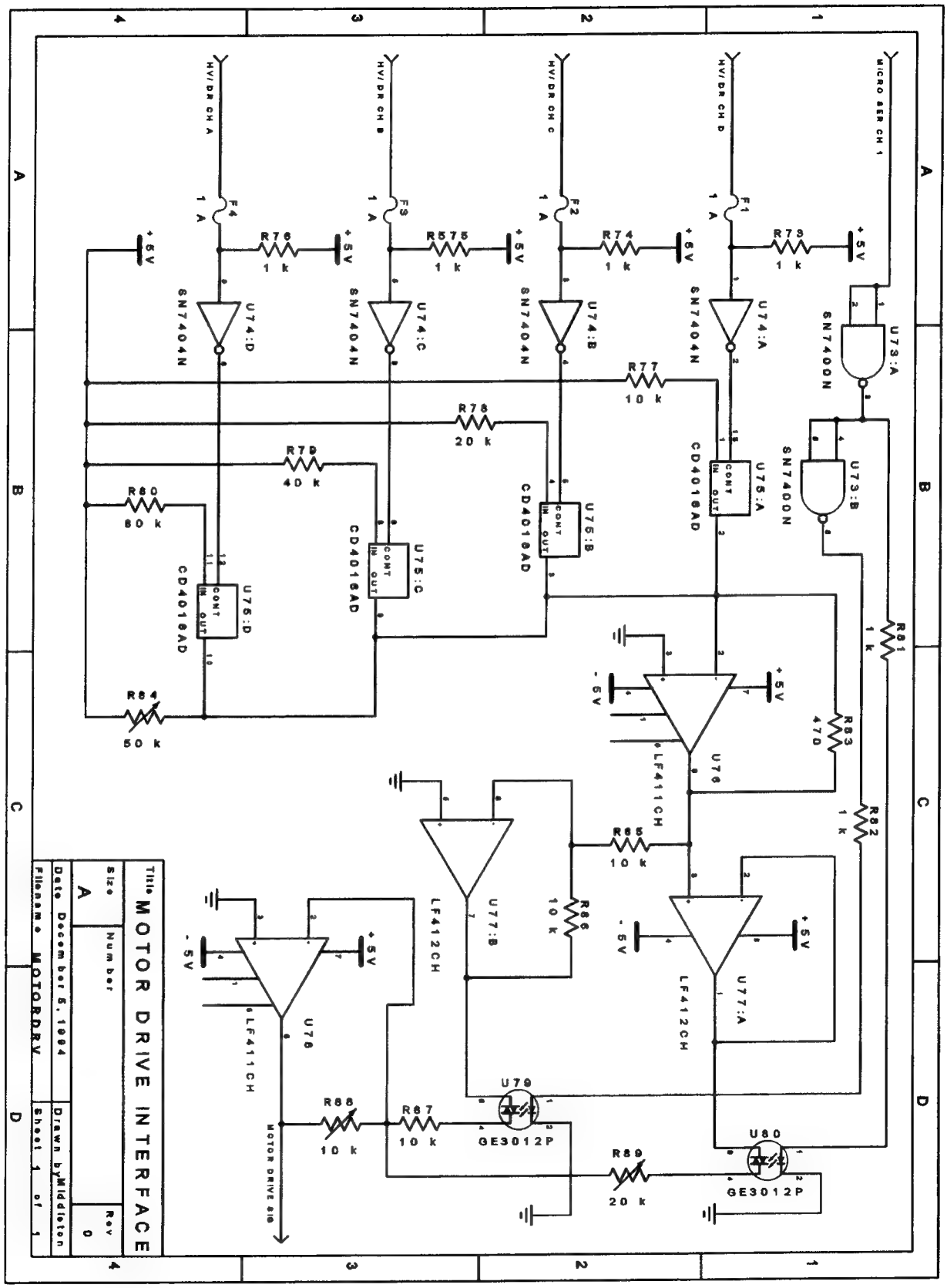

Figure 17. Motor drive circuit.

the output of that channel was high. A sixteen step digital-to-analog converter was made using a quad bilateral switch. An output operational amplifier provides the required gain. A variable resistor provides a reference signal which is also summed by the amplifier. This provides a minimum signal to ensure that even the small level outputs of the microcomputer can drive the motor at a slow speed. After the digital-to-analog subsection, the signal is sent to a unity gain amplifier and an inverting amplifier to yield both positive and negative drive signals. A variable resistor adds a second signal to the inverting amplifier to account for differences in zero drive voltage in running the motor in the forward direction or the reverse direction. The output of the serial channel is used to determine whether the forward of reverse signal is to be sent to drive the motor. A high signal from the serial port will be inverted to form a low signal to an optically coupled MOSFET, which is connected to the unity gain amplifier. The low signal is also sent to an inverter which sends a high signal to an optically coupled MOSFET, which passes the negative drive signal to the motor. When a low signal from the serial port is sent, the MOSFETs act in opposite manner, and the positive drive signal is sent to the motor. An attempt to use quad bilateral switches instead of MOSFETs met with little success due to switch bleed-through.

The outputs of the two MOSFETs are then sent to a final power amplifier. Two variable resistors are provided to allow adjustment to the range of the peak signal provided by the circuitry. This allows for balanced response in both the forward and reverse directions.

c. Motor power amplifier

The motor power amplifier is based on a low distortion design commonly used for acoustic speakers. It uses an LM12 power amplifier and is connected to two 28 volt power supplies. The amplifier is shown in Figure 18. The motor signal is sent to a 9 V, high torque pancake type motor which is capable of high starting torques and fast speeds. The motor/encoder assembly that is rotated is shown in Figure 19.

d. Microcomputer programming

The program used to operate the microcomputer is shown in Appendix A. It consists of a main program that inputs the desired encoder position. The desired position must be

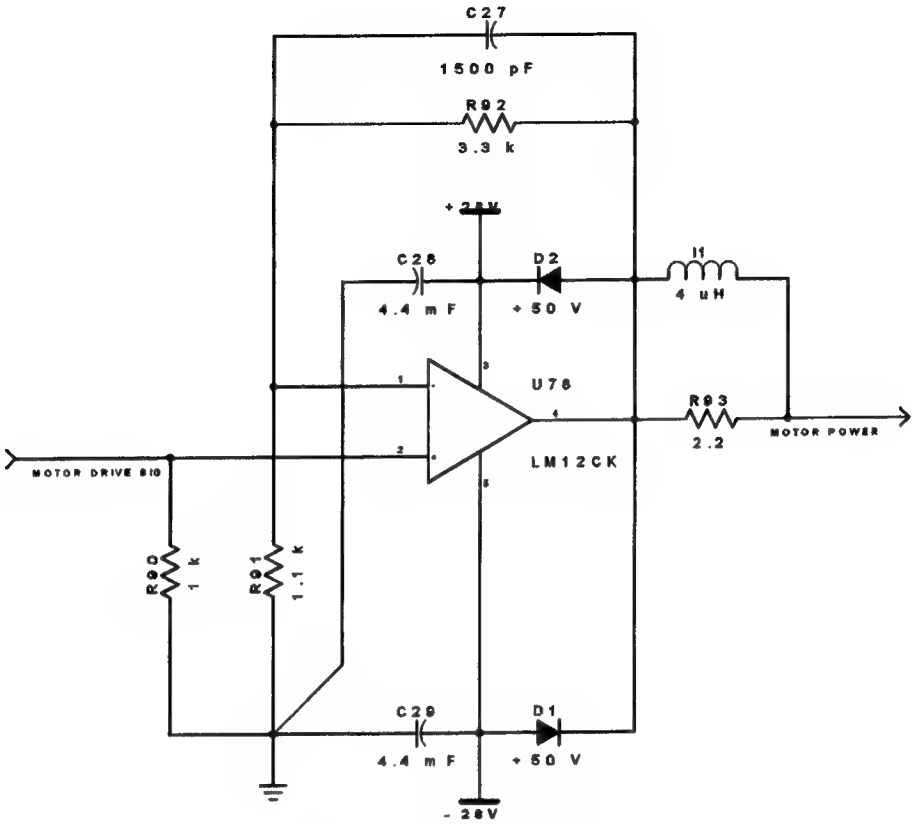

Figure 18. Power amplifier.

input one character at a time using the command GETCHAR(). The program must internally convert the string variables to floating point numbers. As a data type, UNSIGNED LONG INT does not work correctly in Dynamic C. In addition, if all eight input digits were formed to create one floating point number, the number begins to lose accuracy at the fourth significant digit. Therefore, the numbers were left combined in group of no more than three digits. When the number was needed for a calculation, is was reconstituted by multiplying the group of numbers by the value of the least-significant digit's position in the desired number.

The program specifies bit-7 of port B as the interrupt control bit. The interrupt routine is invoked when this bit goes high. On an interrupt, the microcomputer first reads both port A and port B. The microcomputer then switches bit-6 of port B to high to select the B multiplex channels. The microcomputer again reads port A and port B to obtain the 12 most significant bits. The program must be careful to subtract the high logic value from bit 6 of port B from the

received value for port B since the microcomputer has set this bit high and turns around and reads the bit during the input process. Once the position value is read in, it is compared to the requested position and the previous position to form an error signal. The error signal is then checked to see if it is positive or negative and the serial channel set appropriately. Finally, the motor error signal is converted from analog to digital form and sent to the high voltage drivers for output to the circuitry discussed previously in Section III.A.2.b.

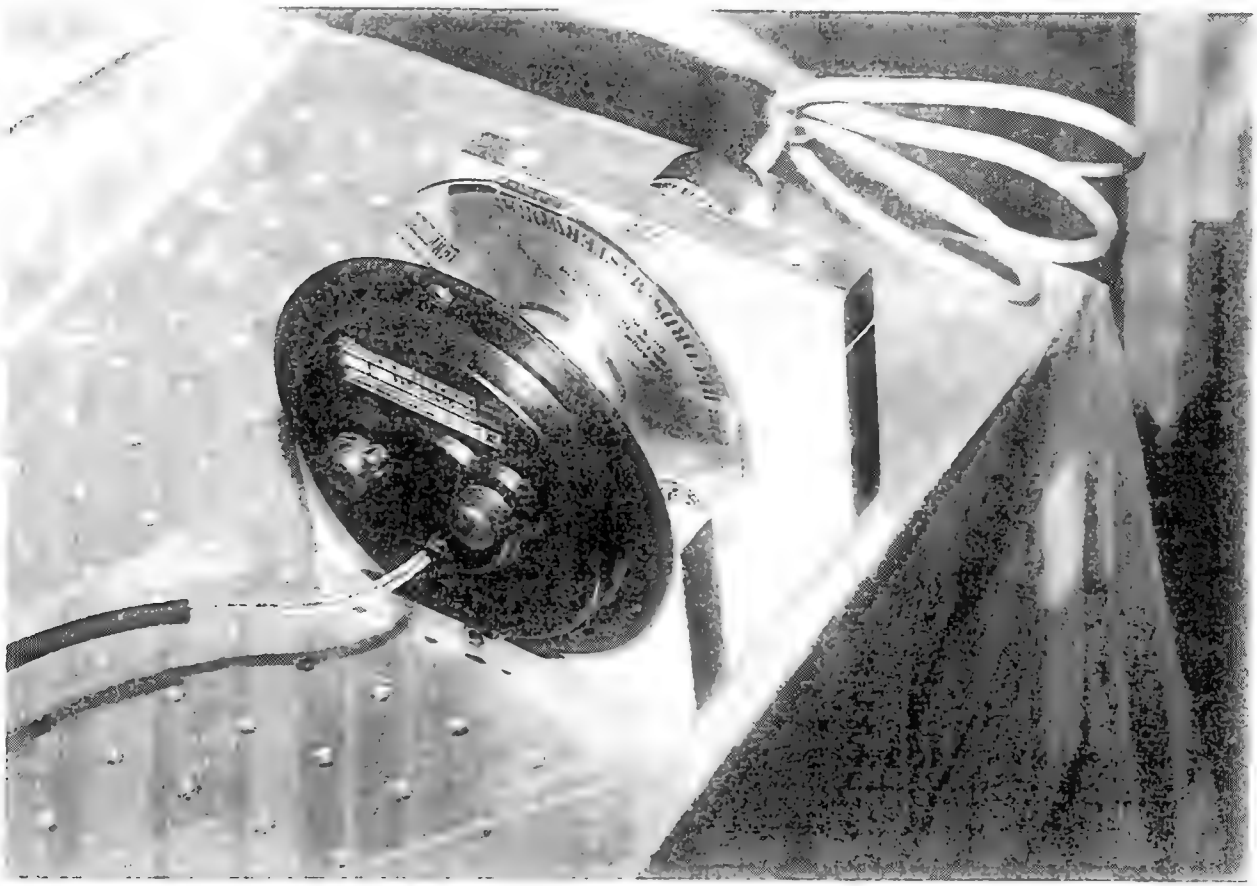

Figure 19. Motor and encoder assembly.

IV. OBSERVATIONS

A. GENERAL

The development process is naturally an interactive combination of design, construction, and redesign. Many observations have already been discussed in Section III as they relate to the design of individual portions of the control system. Other observations are more global in that they relate to the system as a whole. These general considerations are the type that will be discussed in this section.

1. Modulation frequency

When the control system was first operated as a complete unit, testing showed that the motor would start to move the disk, and then would rapidly reach a constant maximum speed. Prior to placing the motor amplifier and motor into the circuit, it was determined, by using an HP4149 impedance analyzer, that the amplifier did not have any poles below 1 MHz. Therefore, instability of the control system was ruled out as a cause. A check of the LCD displays during motor operation showed that the pulse counter was not able to count through a full range of 81,000 waveforms before the Z signal would reset the counter. A computer output check of the pulse counter input also showed that the pulse count was not keeping up with the actual rotation of the encoder. Analysis of the signal waveform at the output of the encoder signals and at the output of the filter revealed two facts:

1) The output period of the encoder signal at the expected maximum operating speed of the motor was 1 μsec. This corresponds to a frequency of 1 MHz. This also corresponds to a motor speed of 740 rpm.

2) Only a very weak signal was detected at the filter output.

These two observations are related. As shown in equation (2), the frequency of the SUM A & B signal is the difference between the modulation frequency and the encoder signal frequency. The difference in frequencies is 900 kHz, which is well above the band-pass filter cutoff frequency

To limit the speed of the motor to ensure that the SUM A & B signal frequency stays within the range of the band-pass filter places a maximum speed limit of 37 rpm on the motor. This option would necessarily lead to longer delay times between measurements. The alternative is to increase the modulation frequency to over 2 MHz and redesign the filter for the new values of $\frac{1}{2}\omega_0$ and $\frac{3}{2}\omega_0$. The CMOS components in the system are capable of handling this higher frequency, but the conflict avoidance circuit would require shortening the triggering pulses (to 40 nsec) and the blanking pulses (to 100 nsec). The limit to the modulation frequency is imposed by the up/down counters. Their maximum propagation delay time is on the order of 40 nsec. Time must be allotted for a minimum of three pulse to propagate through the counters during the period of a reference clock signal. This places an upper bound of 7 MHz for the modulation frequency.

2. Pulse counting vs. phase differentiation

The design of the phase differentiation circuitry calls for the counting of clock pulses between the reference signal pulse (count up) and SUM A & B pulse (count down). Since the limit on the pulse period to the up/down counter is 40 nsec, it would only be possible to fit a maximum of 12 pulses into the time period between the count up pulse and the count down pulse. This limits the phase angle resolution to one-twelfth of a waveform, limiting the positional accuracy of the control system to 6.5 μrad. This does not meet the overall design objectives as stated in the introduction of this thesis. The clock frequency that can obtain maximum phase differentiation is 25 MHz based on propagation limits of the up/down counters.

This observation leads to an important conclusion: **Designing the pulse counting circuit to support rapidly positioning the encoder necessarily requires a trade-off with angular precision.** The same circuit modulating frequency cannot support both high angular velocities and fine angular position precision. When the disk is moving, it is not required to know the position as accurately as when the disk is held steady while the optical measurements are made. It would be possible to design two complete circuits: One circuit to measure both the pulse count and one to differentiate the phase. The pulse counter would run at a higher modulation frequency, and the phase differentiator would run at a lower modulation frequency. The phase differentiator would then be limited in use to only slow motor speeds when final positioning is

desired.

3. Modulator circuit waveform

As discussed in Subsection III.A.1.b, there is a small anomaly in the output waveform of the modulation circuitry. This was considered to be due to the quad analog bilateral switch. Replacing the analog bilateral switches with optically coupled MOSFETs may smooth out the waveform. There was no indication that this anomaly effected operation at 100 kHz modulation frequency, but it could become a more pronounced effect at higher modulation frequencies.

4. Programming "Dynamic C"

Programming the microcomputer proved to be a formidable task. There is little documentation or examples available on how to program the various features of the Tiny Giant. I will list the differences between C and Dynamic C that I found, in hopes that future users will have a historical reference point.

1) Dynamic C does not use #INCLUDE statements. When the C code is compiled, all the necessary library functions are duplicated into the program and compiled with the program just as if you wrote and included those functions in the program yourself.

2) Floating point numbers may not be accurate beyond the third significant digit.

3) The unsigned long integer data type does not work; Numbers greater than 32767 were assigned negative values. Be careful.

4) To enable the serial port, use OUTPORT(EN485,1). This will cause the transmit port to go high. The port will transmit data by pulling itself low to transmit zeroes. The port may be disabled and returned to a ground state (zero) using OUTPORT(EN485,0). Thus, the program can control the output values of the serial channel manually if desired.

5) When using the enable interrupt function after an interrupt is invoked, it is important to place the EI() function first in the interrupt routine. This is contrary to common sense, but prevents problems such as computer time outs for longer running interrupt routines.

6) The only way to interface with the microcomputer once a program is running is the use GETCHAR(). Each time the function is invoked, the keyboard entry is brought into the program as a string. To convert the string to a number, a null character must be placed at the end of the

string and the function atoi() or atof() used. The best way to add the null character is to bring the keyboard entries in as consecutive elements of an array variable and assign the last variable automatically as the null value.

7) To output data on a parallel port designed for some input and some output, write a whole word to OUTPORT(PIOD_,0x__) including the bits you wanted to change. When inputting from that port, you will also include in your input the bits you wrote out. You must keep track of your output bits to subtract from your input.

V PROPOSED ACCURACY EXPERIMENT

A. GENERAL

Although time constraints prevented completion and testing of the control system, much though was put into how to test the accuracy and precision of the system. To meet the design requirements, the control system would have to:

1) Demonstrate an angular position accuracy of less than 1 μrad.
2) Be able to return to the same angular position when requested.
3) Prevent drift from that position.

While it may be easy to measure items 1) and 3) using diffraction techniques; it is the repeatability issue that is the most difficult to determine. An angular change of 1 μrad would deflect a laser beam reflected off a mirror a distance of 0.1 mm off axis 100 meters from the mirror. This is not a feasible technique. The angular change in beam direction is well within both the diffraction-limited beam spread of a typical laser and the acceptable half-angle width for a Fabry-Perot etalon. Therefore, an etalon could not be used.

1. Experimental design

An experiment was designed using a diffraction pattern to provide a laser beam with a substructure perpendicular to the optical axis on the order of 1 μm. The pixels on an open windowed CCD camera would be used to measure angular deflection. The construction of the experiment should proceed as follows: A laser beam is aligned to illuminate an aperture on the order of 1 mm in diameter. A very small lens with a focal length of 1 mm is placed behind the aperture to form a parallel beam of light, thereby generating an Airy diffraction pattern in the Fraunhofer (far-field) regime. Setting the focal length equal to the aperture size ensures fringe diameters in the Airy pattern on the order of 1 μm. The CCD camera is placed at a distance of one meter from a mirror mounted on the edge of the rotating disk. The spacing between the pixels on the CCD camera array are known to be 8 μm. At a distance of 1 meter, beam deflection of 1 μrad must be measured to ensure the proper accuracy. The additional position accuracy on the CCD array is obtained by summing each row of pixels perpendicular to the deflection angle and fitting the values to a distribution curve to determine the position of the centerpoint of the

Airy disk. This method should easily provide resolution on the same order as the substructure of the Airy pattern.

VI CONCLUSIONS

Figure 20 shows a photograph of the completed project. The design of the electronic circuitry appears to be sound, even though time constraints prevented making required modifications to the circuitry to go to the complete testing phase. Following the recommendations in Section IV should make the pulse counter work correctly for the desired positioning speeds. To make further improvements in the accuracy of the apparatus, changes should be made in the mechanical design of the positioning system. Flexible couplings are required when connecting the encoder and the motor to the disk shaft. In addition, a motor with

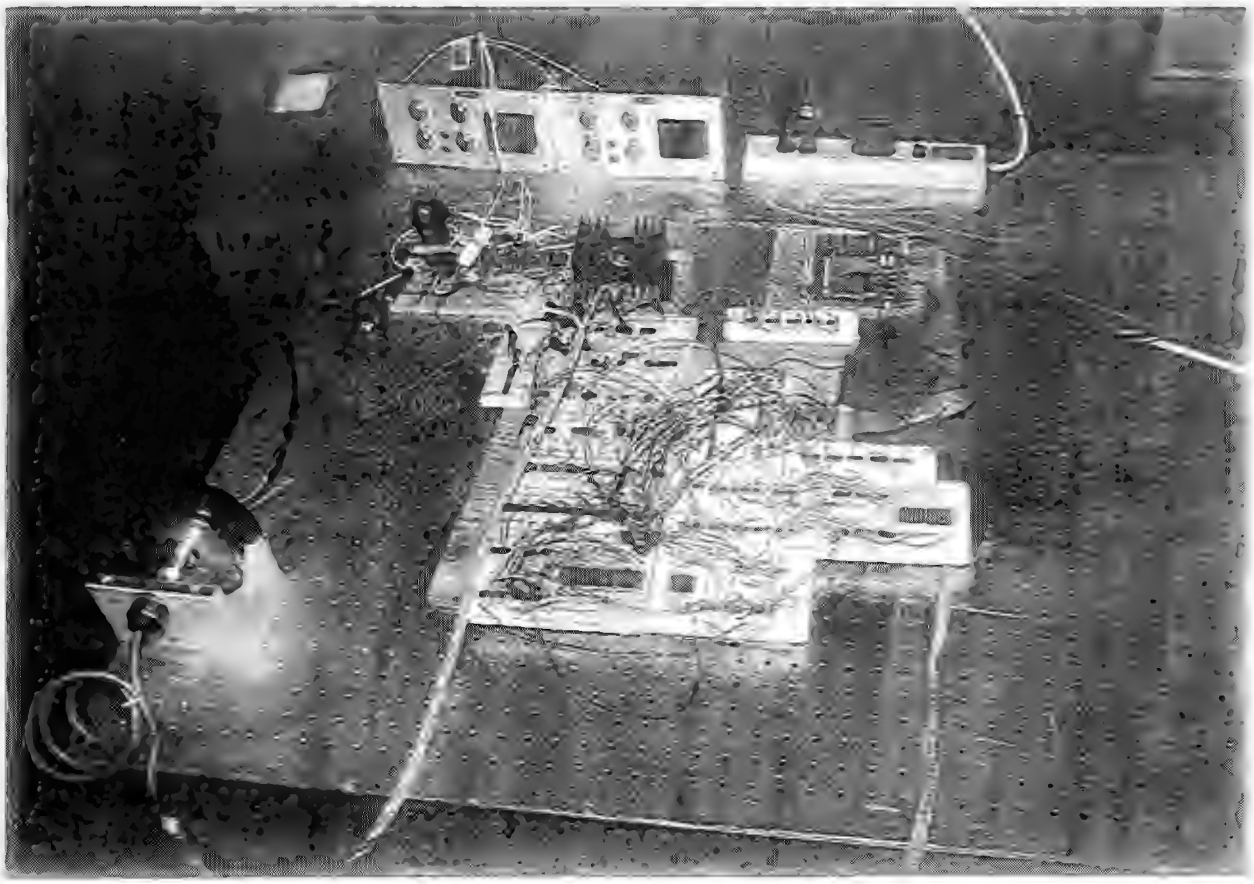

Figure 20. Control system apparatus

smoother starting characteristics will be required to reposition the shaft to within tolerances of 1 μrad when the disk tries to drift from its required position. Finally, I would like to restate the most important observation: High angular velocities, which are needed for fast and efficient positioning of the masks, are inherently incompatible with fine precision in the positioning itself. Additional effort needs to be put into these problem before the design objectives of the multiplexed imager can be realized.

APPENDIX. CONTROL SYSTEM PROGRAM

```
float b,b1,b2,b3,b4;
float v,db,db1,ob,vel_test,vel,motor;
float req1,req2,req3;
char x[4],y[3],z[5];
int count;
int i,j,k,m;
shared float reqa,reqb,reqc;
main(){ b=99999.99;count=0;x[3]=0;y[2]=0;z[0]='.';z[4]=0;
        reqa=0.0;reqb=0.0;reqc=0.0,ob=0.0;
        hv_enb();
        hv_wr(0xa0);
        printf("\n Start rotation.");
        for(j=0;j<1000;j++){;}
        hv_wr(0x00);
        printf("\n Stop rotation.");
  outport(PIOCA,0xff);
  outport(PIOCA,0xff);
  outport(PIOCB,0xff);
  outport(PIOCB,0x7f);
  outport(PIOCB,PIOB_VEC);
  outport(PIOCB,0x97);
  outport(PIOCB,0xbf);
  while(1){
      printf("\n What is the desired next position?");
                  for (i=0;i<3;i++) {x[i]=getchar();}
                  req1=atof(x);
                  y[0]=getchar();y[1]=getchar();
```

```
                    req2=atof(y);
                    for (k=1;k<4;k++) {z[k]=getchar();}
                    req3=atof(z);
                    printf("\n You have requested %fx100 %f %f",req1,req2,req3);
                    reqa=req1;reqb=req2;reqc=req3;
                    printf("\n Actual position is %f",b);
                    printf("\n Position difference is %f",db);
                    printf("\n Motor setting is %d", m);
                    printf("\n Velocity is %f", vel);
                    printf("\n Count is %d.",count);
                if (req1>820.0) {hv_dis(); break;}
            }
    }

#INT_VEC PIOB_VEC INT1

interrupt reti INT1()
{  EI();count++;
        b1=inport(PIODA);
   b2=inport(PIODB); b2=b2-64;
   outport(PIODB,0x80);
   b3=inport(PIODA);
   b4=inport(PIODB);b4=b4-192;
   outport(PIODB,0x00);
   b=16384.0*b4 + 64.0*b3 + b2 + b1/120.0;
        if (b<100000.0) v=1.0; else v=0.0;
db=reqa*100.0+reqb+reqc+100000.0-b-81000.0*v;
if (db>40500.0   'b=db-81000.0;
if (db<-40500.0) db=db+81000.0;
```

```
/*vel_test=b-ob;
if (vel_test<40500.0 && vel_test>-40500.0) vel=vel_test;*/
if (db>0.0) db1=db; else db1=-db;
vel=ob-db;ob=db;
motor=db-vel/db1;
if (motor<0.0) outport(ENB485,1);
                                    else outport(ENB485,0);
motor=abs(motor);
if (motor>15.0) m=15;
                                    else m=(int)motor;
hv_wr(m*16);
  }
```

LIST OF REFERENCES

1. Stein, J., in *The Random House College Dictionary, Revised Edition*, Random House, New York, 1988, ISBN 0-394-43500-1.

2. Harmuth, H. F., *Sequency Theory Foundations and Applications*, Academic Press, New York, 1977.

3. Beauchamp, K. G., *Applications of Walsh and Related Functions, with an Introduction to Sequency Theory*, Academic Press, New York, 1984, ISBN 0-12-084180-0.

4. Davis, D. S., "Multiplexed Imaging by means of Optically-Generated Kronecker Products: 1. The Basic Concept," Submitted for publication in *Applied Optics*, April 1994.

5. Huguenin, B. D., *Design, Development and Testing of a Prototype Optical System for a Next Generation Multiplexed Imager*, Master's Thesis, Naval Postgraduate School, Monterey, CA June 1992.

6. Barbour, C. S., *Prototyping of a Two-beam Laser Interferometer for Measurement of Optical Turbulence Along Extended Paths*, Master's Thesis, Naval Postgraduate School, December, 1992.

7. Stout, D. F., *Handbook of Operational Amplifier Circuit Design*, McGraw-Hill Inc, 1976.

8. Horowitz, P. and Hill, W., *The Art of Electronics*, 2nd ed., Cambridge University Press, 1989.

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